REMARKS

I. Introduction

Applicants have amended claims 11 and 14 in accordance with the recommendation made by the Examiner during a telephone conversation which took place at or around March 6, 2006. The amendments indicate that the semiconductor substrate is comprised of a semiconductor material. Support for the amendment to claims 11 and 14 may be found, for example, on page 15, lines 8-18. In addition, claim 15 has been amended to further clarify the present invention. No new matter has been added.

Applicants note with appreciation the indication of allowable subject matter being recited by claims 13 and 16.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection of Claims 11, 12, 14 and 15 Under 35 U.S.C. § 102

Claims 11, 12, 14 and 15 were rejected under 35 U.S.C. § 102 as being anticipated by Yamamura (U.S. 5,341,096). Applicants respectfully submit that Yamamura fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, amended claims 11 and 14 both recite, in-part, a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material having a wiring layer.

Yamamura discloses an LSI mounted on a printed circuit board 6 (col. 2, lines 14-18, Fig. 5). However, it is clear that the printed circuit board is not composed of a semiconductor

material, and therefore cannot be deemed a semiconductor wiring substrate being composed of a semiconductor material. Thus, Yamamura fails to disclose at a minimum, a semiconductor device comprising a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material having a wiring layer, as recited by claims 11 and 14 of the present invention.

Furthermore, claim 11 discloses in part, an internal scan chain for an internal scan test provided in each of said chip IPs, wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing respective scan tests simultaneously with each other, using test data which is input from outside.

Yamamura also discloses that the boundary scan test circuit and the internal scan chain are capable of operating simultaneously with each other. However, all test data inputted to the boundary scan test circuit and the internal scan chain during the above simultaneous operation are pseudo random patterns since the object of the invention disclosed in Yamamura is to perform burn-in tests, and not scan tests. Thus, Yamamura fails to disclose an internal scan chain wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing respective scan tests simultaneously with each other.

Moreover, claim 14 recites, in-part, a semiconductor device comprising: at least two pieces of wiring for inputting test data directly from outside to or outputting a test result directly to outside from said boundary scan test circuit of at least one of said chip IPs, said at least two pieces of wiring being formed in the wiring layer of said semiconductor wiring substrate to be used only for testing.

In contrast, Yamamura fails to disclose that the structure where wiring for testing is for only scan testing and the respective chip IPs bonded on the wiring substrate can be directly scan tested from outside. Thus, Yamamura fails to anticipate claim 14 of the present invention as well.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and at a minimum, Yamamura does not disclose a semiconductor device comprising a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material having a wiring layer, OR an internal scan chain wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing respective scan tests simultaneously with each other, OR at least two pieces of wiring for inputting test data directly from outside to or outputting a test result directly to outside from said boundary scan test circuit of at least one of said chip IPs, said at least two pieces of wiring being formed in the wiring layer of said semiconductor wiring substrate to be used only for testing, it is clear that Yamamura does not anticipate either of claims 11 and 14, or any claim dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 11 and 14 are patentable for the

reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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